Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated February 17, 2004 indicated that claims 29-31, 33 and 34 stand objected to but indicated to be allowable if rewritten in independent form with limitations of the base claim and any intervening claims; claim 1 stands rejected under 35 U.S.C. § 103(a) over *McCaslin* (U.S. Patent No. 5,668,794) in view of *Barron et al.* (U.S. Patent No. 5,357,567); claim 2 stands rejected under 35 U.S.C. § 103(a) over the '794 reference in view of the '567 reference and further in view of *Chen et al.* (U.S. Patent No. 5,075,687); claim 4 stands rejected under 35 U.S.C. § 103(a) over the '794 reference in view of the '567 reference and the '687 reference and further in view of *Teitler et al.* (U.S. Patent No. 5,722,086); claims 7-8 stand rejected under 35 U.S.C. § 103(a) over the '794 reference in view of the '567 reference and further in view of the '086 reference; claim 9 stands rejected under 35 U.S.C. § 103(a) over the '794 reference in view of the '567 reference and the '086 reference and further in view of Intel (80C186EA/80C188EA Microprocessor User's Manual) (hereinafter the "Intel" reference); and claims 24, 26-28 and 35 stand rejected under 35 U.S.C. § 103(a) over the '794 reference in view of the '086 reference.

Applicant respectfully traverses the Section 103(a) rejections (as applicable to all rejected claims) over the '794 (McCaslin) reference in view of the '567 (Barron) reference because the Examiner failed to establish a *prima facie* case of obviousness. *See* M.P.E.P. §706.02(j). Specifically, the Examiner failed to show correspondence between the cited portions of the references and all of the claimed limitations, and further failed to provide any evidence of motivation for modifying the '794 reference. In addition, the proposed modification of the '794 reference would undermine its purpose of implementing its variable gain algorithm and of providing full-duplex processing (thus the proposed modification is unmotivated).

In direct contrast to the teachings of the claimed invention, the Examiner has made a hypothetical "prior art" combination of references that would replace the algorithm and approach of the '794 reference with a microprocessor-implemented approach that directly undermines the purpose of the '794 reference. Specifically, the

purpose of the '794 reference involves using a particular variable gain algorithm for implementing echo suppression. *See, e.g.*, column 27, line 66 through column 28, line 12. The Examiner's suggestion that a skilled artisan would be motivated to replace the algorithm and corresponding circuit components of the '794 reference with the microprocessor-implemented approach of the '567 reference is therefore untenable. Moreover, the proposed modification of the primary '794 reference does not address the shortcomings of the '794 reference because the asserted combination still fails to teach or suggest claimed limitations including alternately receiving speech signals in respective speech paths, as well as full duplex operation. The following discussion refers back to the above-described "hypothetical prior art" proposed by the Examiner.

In an apparent attempt to overcome the deficiencies of the '794 reference relative to the claimed limitations of the instant invention, the Examiner simply stated that the "microprocessor, memories and algorithm storage taught by Barron" could be applied to the echo suppressor taught by the '794 reference. In addition, the Examiner further asserted, on page 4 of the Office Action, that the receipt of a speech signal on each speech path during each sample period with the '794 reference implies alternately receiving speech signals as claimed. However, as previously discussed, the Examiner has not shown how the '794 reference would be modified to include these limitations and thus has not shown how all of the cited elements would work together as claimed. For example, adding the "microprocessor, memories and algorithm storage taught by Barron" to the '794 reference would maintain the same operation taught by the '794 reference and thus does not provide correspondence to the claim limitations (*e.g.*, alternately receiving speech signals) of the present invention.

More particularly, the Examiner has cited no portion of the '794 reference that would indicate that the receipt of a speech signal on each speech path during a sample period implies, as the Examiner asserts, alternately receiving speech signals, or that a microprocessor-implemented approach is contemplated. Rather, the sampling of speech signals in the incoming and outgoing speech paths in the '794 reference is concurrent and implemented with discreet components. There is no discussion in the cited portions of the '794 reference that would indicate that speech signals in different speech paths are alternately received. In addition, the algorithm of the '794 reference is implemented with

discreet components as described, for example, in connection with FIG. 19. For instance, the cited portions of the '794 reference discussing the embodiments shown in FIG. 19 rely upon the double-talk detector 54 and adaptive filter 40 of FIG. 1 for implementing the echo canceller 408 (*see, e.g.,* column 21, lines 30-35). The double-talk detector 54 is further discussed in connection with FIG. 2, and the adaptive filter 40 with FIG. 6, with reference to various discreet component implementations. Furthermore, in absence of a microprocessor and in view of the purposeful discrete circuit implementations discussed above, clearly the discreet approach of the '794 reference would involve the simultaneous sampling of speech signals in alternate paths. For instance, referring to FIG. 20, discrete peak detect circuits 420 and 428 are separately implemented and simultaneously sample signals in different speech paths; there is no teaching or suggestion of coordination between these discrete components. In this regard, the Examiner has not shown how the cited references teach all of the claim limitations and thus has failed to meet the correspondence requirement for establishing a *prima facie* Section 103 rejection.

The Examiner further failed to cite any evidence in support of the assertion that the proposed modification of the '794 reference would be motivated. Specifically, the Examiner asserted that, because the purpose of the modification is to implement "the echo suppressor in a physical platform," one of skill in the art would be motivated to do so. These mere allegations of motivation made in hindsight and without any supporting evidence do not meet the evidence requirement for establishing a *prima facie* Section 103 rejection. *See, e.g., In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). *See also In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (evidence of teaching or suggestion "essential" to avoid hindsight). In this instance, the Examiner's conclusion that one of skill in the art would look to modify the '794 reference in this manner lacks evidence that would show why one of skill in the art would be motivated to embody the echo suppressor in the manner suggested by the Examiner. Therefore the Section 103 rejection fails to meet the motivation requirement for establishing a *prima facie* Section 103 rejection.

Moreover, the proposed modification would undermine the purpose of the relied-upon embodiment of the '794 reference of achieving full-duplex operation while maintaining low-cost. *See, e.g.*, column 3, lines 30-37 and column 7, lines 10-23. Where

a proposed modification of a primary reference would undermine its purpose, there is no motivation to make the modification (*see, e.g.*, *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984)). The Applicant has previously pointed out that the '794 reference has a purpose of low-cost implementation, in referencing the drawbacks of previous implementations of echo cancellation with an adaptive filter. The Examiner has pointed out, in the Response to Arguments section, that the '794 reference indeed uses a filter in certain embodiments. However, the Applicant has not asserted that this purpose of the '794 reference requires that no adaptive filter be used. Rather, the above-referenced portions of the '794 reference emphasize the reference's purposes of achieving full-duplex operation at low cost. While the '794 reference does employ an adaptive filter as pointed out by the Examiner, the implementation of the filter is effected in connection with this purpose, which would be undermined, were the proposed combination made.

Regardless of whether the '794 reference employs an adaptive filter, the addition of the expensive programmed '567 processor (DSP56001), as well as the '567 memory circuit and its algorithm storage to the '794 reference would be contrary to the purpose of the '794 reference. The '794 reference teaches the utilization of the algorithm described at column 12, line 64 through column 13, line 14, with discrete circuitry (without a processor) being used to address the high speed data processing required to suppress the echo. In this regard, the Examiner's comments on page 15 in the Response to Arguments section of the Office Action, indicating the Applicant has no support for utilizing the algorithm with discrete circuitry, are incorrect. The cited portion of the '794 reference discussed by the Examiner refers to another U.S. Patent Application that involves the use of such discrete circuits. Furthermore, as discussed above, various other cited portions of the '794 reference specifically call out the use of discrete circuitry.

Inserting the programmed '567 processor (DSP56001) as well as the '567 memory circuit and its algorithm storage into the heart of the '794 system would result in a much more expensive '794 system as well as replace this '794 circuitry and algorithm. It is also unclear as to whether the '794 system would operate as intended, were its circuitry and algorithm replaced; the Examiner has not shown how this replacement would function. Furthermore, the new half-duplex-switching algorithm of the '567 reference would destroy the full-duplex purpose of the '794 reference. This proposed

modification of the '794 reference would thus undermine its purpose and therefore is unmotivated.

In view of the above, the Examiner failed to show correspondence between the cited references and all of the claimed limitations, failed to provide evidence in support of the asserted modification of the '794 reference and relies upon a proposed modification that would undermine the purpose of the '794 reference. Therefore, Appellant submits that a *prima facie* Section 103 rejection has not been established and requests that the rejection be removed.

Each of the remaining rejections is further traversed for reasons stated above regarding the deficiencies of the '794 reference in its failure to correspond to various claimed limitations. Claims 2, 4 and 7-9 are further traversed for the reasons stated above regarding the impropriety of the combination of the '567 reference with the '794 reference. Notwithstanding the above, however, Applicant has further addressed selected ones of the claim rejections below.

Regarding the Section 103 rejection of claim 2, Applicant submits that the Examiner failed to show correspondence between the cited references and every limitation in claim 2. For example, the Examiner asserts on page 5 of the Office Action that the "analog-to-digital and digital-to-analog converter combination" in FIG. 19 of the '794 reference constitutes a codec. However, the Examiner failed to show how this combination corresponds to the claimed limitations directed to a codec "having first and second programmable digital attenuators" in claim 2. Therefore, the Examiner failed to meet the requirement that all limitations be taught in order to establish a *prima facie* Section 103 rejection, and Applicant requests that the rejection be removed.

Further regarding the Section 103 rejection of claim 2, Applicant submits that the Examiner failed to cite evidence of motivation for making the asserted modifications of the primary '794 reference. Instead of citing evidence, the Examiner has made allegations of motivation in hindsight and without any support for the allegations. For example, on page 5 of the Office Action, the Examiner discusses that it "would have been obvious" to apply integration for "reducing cost and improving stability, sensitivity and consistency." On page 6 of the Office Action, the Examiner further discusses that adding a booster amplifier would have been obvious for "creating a better quality transmitted

signal...." As discussed above, without evidence in support of such allegations, there is no *prima facie* case for maintaining a Section 103 rejection and Applicant therefore requests that the rejection be removed.

Regarding the Section 103 rejection of claims 8 and 9, the Examiner has also failed to show correspondence between the cited references and all claimed limitations. For example, the Examiner has failed to show where any reference teaches or suggests limitations directed to a software timer that generates a hardware interrupt on every speech frame so that a hands-free register can be read by a software peak detector. While the Examiner has mentioned, on page 8 of the Office Action, that the '794 reference discloses the use of software timers, the cited portion of the '794 reference does not disclose software times. In addition, the Examiner has not shown how this cited portion would correspond to other cited portions of the '794 reference that allegedly teach other claimed limitations including peak detection and determination of peak speech amplitude over predetermined sample times. Furthermore, the Examiner has failed to provide evidence of motivation for combining the multitude of references strung together to arrive at the alleged teachings. In attempting to show evidence of such motivation, the Examiner simply stated asserted advantages for the various secondary references and failed to provide evidence showing specifically why the primary '794 reference should be modified or why it would benefit from such alleged advantages. Without showing correspondence to all claimed limitations or proper evidence for modifying the '794 reference, there is no *prima facie* Section 103 rejection for claims 8 and 9 and Applicant requests that the rejection be removed.

With respect to the Section 103 rejection of claims 24 and 35 over the '794 *McCaslin* reference in view of *Teitler*, Applicant respectfully traverses because the asserted prior art does not correspond to the claimed invention. The '794 reference is deficient in alleged teachings as discussed above in connection with the Section 103 rejection of claim 1 (and others having similar limitations). For instance, the cited portion of the '794 reference allegedly teaching limitations directed to "determining regularly the respective peak amplitudes of signals" fails to mention peak amplitude determination. In addition, the '794 reference has been misinterpreted as having an echo

suppressor 414 that must alternately receive speech signals, respectively, in transmit and receive paths. Rather, the echo suppressor 414 of figure 19 of the '794 reference is shown and described in enlarged form via figure 20. In connection with figure 20, the '794 reference describes and illustrates the far end and near end portions of the echo suppressor 414 as being implemented in discrete paths and without any alternate signal receiving or other alternate processing. Thus, in view of this misinterpretation being applicable to each of claims 24 and 35 (as well as their dependent claims), Applicant requests that this rejection also be removed.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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